

# Investigation of Defects Origin in *p*-Type Si for Solar Applications

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In order to improve the efficiency of a solar cell based on silicon, one must find a compromise between its price and crystalline quality. That is precisely why the knowledge of defects present in the material is of primary importance. This paper studies the defects in commercially available cheap Schottky titanium/gold silicon wafers. The electrical properties of the diodes were defined by using current–voltage and capacitance–voltage measurements. Low series resistance and ideality factor are proofs of the good quality of the sample. The concentration of the acceptors is in accordance with the manufacturer's specifications. Deep level transient spectroscopy measurements were used to identify the defects. Three hole traps were found with activation energies equal to 0.093 eV, 0.379 eV, and 0.535 eV. Comparing the values with the available literature, the defects were determined as connected to the presence of iron interstitials in the silicon. The quality of the silicon wafer seems good enough to use it as a substrate for the solar cell heterojunctions.

**Key words:** Solar cells, silicon, defects, DLTS

## INTRODUCTION

First-generation solar cells based on a monocrystalline silicon still dominate the photovoltaic (PV) market. However, in order to make solar energy more accessible and profitable for both industry and private consumers, their prices must be lowered. At the same time, efforts are being made to integrate silicon substrates with thin films or nanostructures to introduce cheap third-generation solar cells.<sup>1,2</sup> The cost of the material is directly related to its purity and crystalline quality. Nevertheless, materials of very low quality are not suitable for solar applications due to the defects affecting the performance of the solar cells. In order to improve the efficiency of a solar cell, one must find a satisfactory

compromise between its price and its crystalline quality.

Solar cells based on *n*-type zinc oxide nanorods and *p*-type silicon have recently been developed.<sup>3,4</sup> Cheap silicon wafers have been used as a substrate to lower the production costs. Once the properties of the material are characterized, further optimization of the heterojunctions will be possible. The presence of defects is always undesirable, particularly the presence of those which can act as recombination centers and mediate in dark current transport (recombination, trap-assisted tunneling, etc.). In effect, both the quantum efficiency and the efficiency of a solar cell decrease. Therefore, the recognition of the defects (and related carrier traps) and their characterization is of crucial importance for optimizing the solar cell structure. That is why the knowledge of defects present in the material is of primary importance. This paper studies the defects in commercially available cheap Schottky

(Received September 26, 2016; accepted March 7, 2017;  
published online March 24, 2017)

titanium/gold silicon wafers. The electrical properties of the diodes were defined by means of current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) measurements. Deep level transient spectroscopy (DLTS) measurements were used to characterize the defects.

## EXPERIMENTAL

*p*-Type silicon wafers with the resistivity of 2 Ωm, thickness of 200 μm and orientation (100) were cut into 1 × 1 cm<sup>2</sup> pieces. They were cleaned for 5 min in 2-propanol, acetone and deionized water in an ultrasonic cleaner. On top of the sample bar, a Schottky contact of Ti(15 nm)/Au(40 nm) was deposited using e-beam evaporation (PVD 75; Kurt Lesker). The bottom aluminum ohmic contact was deposited in the same system. Gold wires were bonded to the contacts using Kulicke & Soffa 4700 Manual Analog Wire Bonder. *I*–*V* characteristics were measured using a Keithley 2601A. *C*–*V* characteristics were performed by using a Boonton 7200 capacitance meter. The DLTS spectra were produced by using a lock-in system based on the same capacitance meter. In order to achieve temperatures down to 80 K, the samples were placed inside a Janis helium cryostat system.

## RESULTS AND DISCUSSION

### Current–Voltage Characteristics

The measurements of the *I*–*V* characteristics allows the obtaining of the basic parameters of the junction as well as the determining of its quality. The dark room temperature characteristic for the studied Schottky contact is presented in Fig. 1. The junction exhibits good rectifying properties. It is possible to perform the DLTS measurements on this diode.

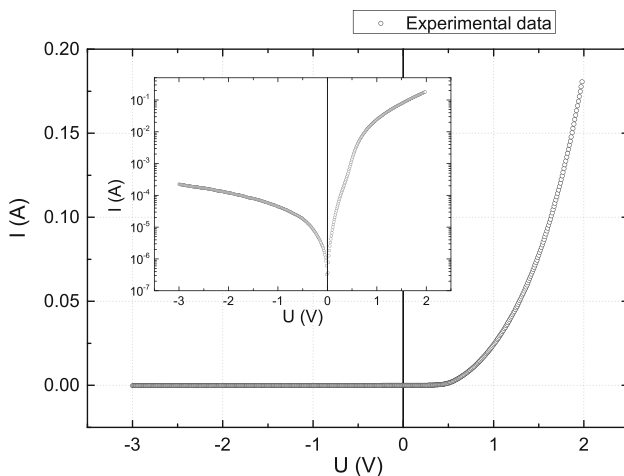


Fig. 1. *I*–*V* characteristic for the Schottky junction. Inset the same plot in the half-logarithmic scale.

According to the thermionic emission model, the current transport at a lower voltage bias can be given as<sup>5</sup>:

$$I = I_0 \exp\left(\frac{qV}{nkT} - 1\right) \quad (1)$$

where *q* is the electronic charge, *V* is the forward voltage bias, *n* is the diode ideality factor, *k* is the Boltzmann's constant, *T* is the absolute temperature and *I*<sub>0</sub> is the reverse saturation current. The saturation current is given by<sup>5</sup>:

$$I_0 = AA^* \exp\left(-\frac{q\Phi_B}{kT}\right) \quad (2)$$

where *A* is the diode contact area, *A*<sup>\*</sup> is the effective Richardson constant and equals 32 A/(cm<sup>2</sup> K<sup>2</sup>) for *p*-type Si,<sup>6</sup>  $\Phi_B$  is the effective barrier height at a zero voltage bias. The saturation current *I*<sub>0</sub> can be calculated by extrapolating the linear line to a zero applied voltage bias. In the next step, the barrier height may be determined from Eq. 2. The ideality factor can be calculated from the slope of the linear part of the forward bias ln(*I*) versus *V* plot and can be written from Eq. 1 as:

$$n = \frac{q}{kT} \left( \frac{dV}{d(\ln I)} \right) \quad (3)$$

The basic junction parameters obtained from Fig. 1 are collected in Table I. The series resistance is low,<sup>7,8</sup> which allows one to conclude that the quality of the junction is good. The ideality factor is between 1 and 2, which means that the current is limited by the recombination of minority carriers as well as majority carriers.

### Capacitance–Voltage Characteristics

DLTS studies are usually preceded by *C*–*V* measurements. In Fig. 2, the room-temperature *C*–*V* curve is presented. The inset shows  $A^2/C^2 = f(U)$ , where *A* is the area of the Schottky contact. The linear approximation of this curve allowed us to calculate the acceptors' concentration (*N*<sub>A</sub>) and the built-in voltage (*V*<sub>bi</sub>) by using the standard equation<sup>6</sup>:

$$\frac{A^2}{C^2} = \frac{2}{qN_A \epsilon_0 \epsilon_s} (V_{bi} + U), \quad (4)$$

Table I. Parameters obtained from *I*–*V* characteristics presented in Fig. 1

<i>R</i> <sub>s</sub> (Ω)	<i>I</i> <sub>0</sub> (A)	<i>n</i>	$\Phi_b$ (eV)
3.4	$8 \times 10^{-7}$	1.63	0.66

*R*<sub>s</sub> series resistance, *I*<sub>0</sub> saturation current, *n* ideality factor,  $\Phi_b$  potential barrier.

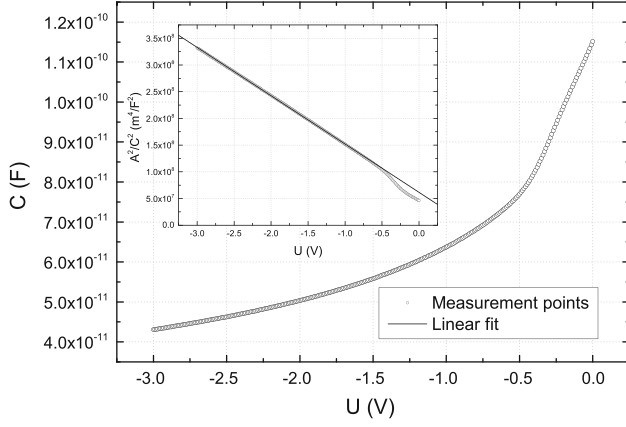


Fig. 2. Capacitance–voltage characteristics. Inset the plot of  $A^2/C^2 = f(U)$ , from which the basic parameters were obtained.

**Table II. Parameters obtained from the C–V characteristics presented in Fig. 2**

$N_A$ (cm <sup>-3</sup> )	$V_{bi}$ (V)	$E_F$ (eV)	$\Phi_b$ (eV)
$1.3 \times 10^{15}$	0.67	0.22	0.89

$E_F$  the energy of the Fermi level.

where  $q$  is the elementary charge,  $\epsilon_0$  the vacuum permittivity, and  $\epsilon_s = 11.7$ , the relative permittivity of silicon. The parameters obtained from the fitting are listed in Table II.

The concentration of the acceptors is in accordance with the manufacturer's specifications. The value of barrier height  $\Phi_b$  obtained from the C–V measurements is higher than the value obtained from the I–V characteristics. Such a tendency is usually observed for inhomogeneous Schottky contacts.<sup>9</sup> The current through an inhomogeneous Schottky barrier is dominated mainly by the low-barrier height, but the C–V behavior is dominated by the barrier height with the largest contact area. Thus, a higher  $\Phi_b$  (C–V) than  $\Phi_b$  (I–V) is finally predicted.

The energy of the Fermi level was obtained from the formulae<sup>6</sup>:

$$E_F = \frac{kT}{q} \ln \frac{N_V}{N_A}, \quad (5)$$

where:

$$N_V = 4.83 \times 10^{15} T^{3/2} \left( \frac{m^*}{m_0} \right)^{3/2} [\text{cm}^{-3}] \quad (6)$$

where  $N_V$  is the density of states at the top of the valence band and equals  $1 \times 10^{19} \text{ cm}^{-3}$ . The potential barrier was then calculated from the formula<sup>6</sup>:

$$q\Phi_b = qV_{bi} + |E_F| \quad (7)$$

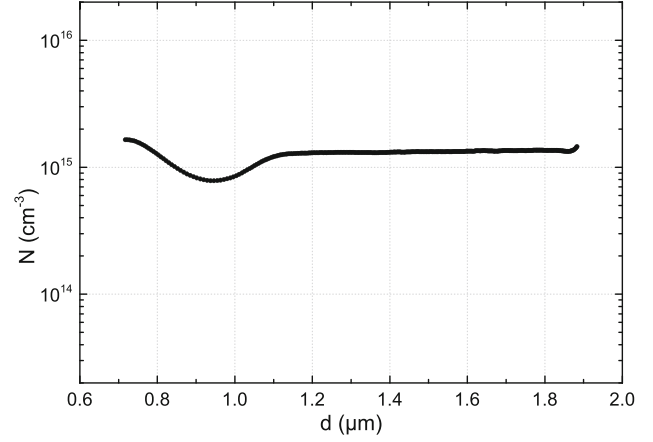


Fig. 3. Free carriers concentration obtained from the C–V characteristics presented in Fig. 2.

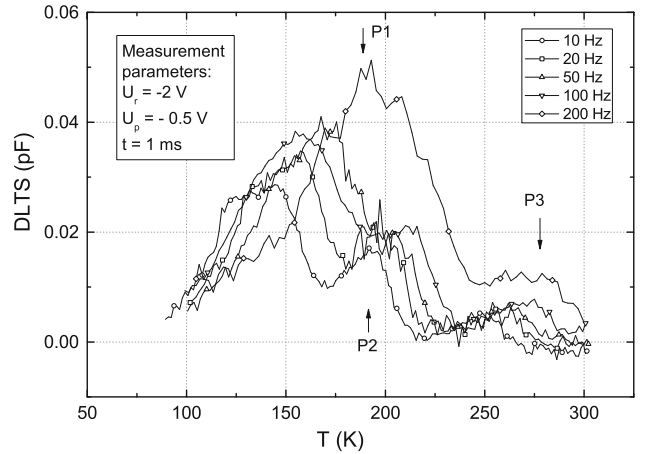


Fig. 4. The DLTS spectra for the Schottky junction measured for different lock-in frequencies.  $U_r$  reverse bias voltage,  $U_p$  pulse voltage,  $t$  filling pulse duration.

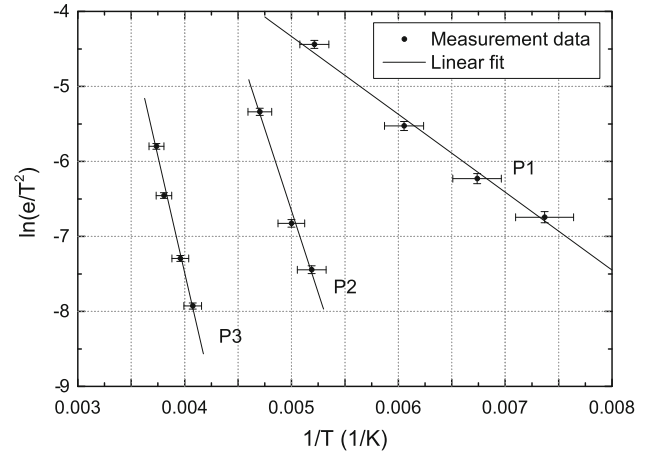


Fig. 5. Arrhenius plots obtained from DLTS spectra presented in Fig. 3.

**Table III. The parameters of the defects' levels obtained from the Arrhenius plots presented in Fig. 4**

Peak	$E_a$ (eV)	$\sigma$ (cm <sup>2</sup> )	$N_t$	Identification
P1	$0.093 \pm 0.067$	$(2 \pm 1) \times 10^{-21}$	$0.2\% N_A$	$E_a = 0.095$ eV Fe-B <sup>11</sup> $E_a = 0.1$ eV Fe <sup>12</sup>
P2	$0.379 \pm 0.042$	$(3 \pm 1) \times 10^{-15}$	$0.08\% N_A$	$E_a = 0.39$ eV Fe-B <sup>12</sup> $E_a = 0.35$ eV transition metals <sup>13</sup>
P3	$0.535 \pm 0.039$	$(3.0 \pm 0.5) \times 10^{-15}$	$0.04\% N_A$	$E_a = 0.525$ eV $\sigma = 5 \times 10^{-15}$ cm <sup>2</sup> Fe-B <sup>14</sup>

$E_a$  activation energy of the defect,  $\sigma$  apparent capture cross-section,  $N_t$  concentration of the traps.

and is presented in Table II.

Figure 3 shows the free carriers concentration ( $N_{cv}$ ) versus the depth of the depletion region ( $d$ ). The values presented on the plots were obtained from the formulae<sup>6</sup>:

$$d = \sqrt{\frac{2\epsilon_s\epsilon_0}{qN_A}}(V_{bi} + U) \quad (8)$$

$$N_{cv}(d) = -\frac{C^3}{A^2 q \epsilon_s \epsilon_0 \left(\frac{dC}{dU}\right)} \quad (9)$$

The free carrier is almost constant within the whole depletion region of the examined Au/Ti-Si Schottky contact. The drop of the concentration near the surface of the sample may be caused by the diffusion of the hydrogen to the silicon.<sup>10</sup>

### DLTS Measurements

The DLTS measurements were performed to obtain the parameters of the deep traps related to the defects present in the silicon wafer. Figure 4 presents the spectra measured at different lock-in frequencies. The parameters of the measurements are given on the plot. The analysis of the  $C$ - $V$  characteristics was used to settle the reverse bias voltage as well as the filling pulse voltage.

The spectra consist of three peaks. The Gaussian fitting was made to obtain the temperature of the maximum signal of the peak. The obtained data were used to prepare the Arrhenius plots presented in Fig. 5. From the linear fitting of those plots, the apparent activation energy and capture cross-section were obtained using the formulae:

$$\ln\left(\frac{e}{T^2}\right) = \ln(A\sigma) - \frac{E_a}{kT} \quad (10)$$

$$A = 2\sqrt{3}M_C(2\pi)^{\frac{3}{2}}k^2 m^* h^{-3}, \quad (11)$$

where  $M_C$  is the number of the minima in the conduction band,  $m^*$  is the effective hole mass, and  $h$  is the Planck constant.

The concentrations of the traps ( $N_t$ ) were calculated knowing the maximum of the signal of the

peaks ( $\Delta C$ ) and the capacitance at the voltage, which was the same as the reverse bias voltage during the DLTS measurements ( $C_{Ur}$ ), following the formula<sup>6</sup>:

$$\frac{\Delta C}{C_{Ur}} = \frac{N_t}{2N_A}. \quad (12)$$

The obtained parameters are shown in Table III.

Three hole traps were found. The deep traps P1 and P2 with activation energies of 0.093 eV and 0.379 eV, respectively, have been observed by other authors.<sup>11</sup> The low energy trap occurs along with the deeper one, and they are both associated with the iron interstitial (Fe<sub>i</sub>). The concentrations of those traps is lower than reported by the authors. This can prove the good quality of the Si wafer.

In Ref. 13, the authors observed a trap with a signature close to the signature of trap P3 (0.535 eV). It was connected to the presence of impurities, such as transition metals in the silicon.

### CONCLUSION

In this paper, silicon Schottky junctions for solar applications were characterized by means of electrical measurements. The parameters obtained from the  $I$ - $V$  curves confirm the good quality of the diodes. The  $C$ - $V$  characteristics made it possible to obtain the concentration of the acceptors and the potential barrier, which are in accordance with the manufacturer's data and the literature, respectively. The DLTS measurements revealed the presence of three defects. They were found as related to the transition metals, specifically iron interstitials.

The measurements performed indicate the good quality of the silicon. The rectifying properties of the Schottky junction are good and the concentrations of the found traps are low. Therefore, the wafer is suitable as a substrate in thin film solar cells.

### ACKNOWLEDGEMENTS

This work has been partially supported by the statutory grant Wroclaw University of Technology, S50013, by the National Science Centre (Decision Nos. DEC-2012/06/A/ST7/00398 and DEC-2013/11/B/ST7/01385). Author K.G. would like to acknowl-

edge the financial support in the form of a scholarship from a special-purpose grant awarded to Faculty of Fundamental Problems of Technology by Ministry of Science and Higher Education in 2016 for research and development of young scientists and Ph.D. students.

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